Beyond Transistor Scaling:

New Devices for Ultra-Low-Energy Information Processing

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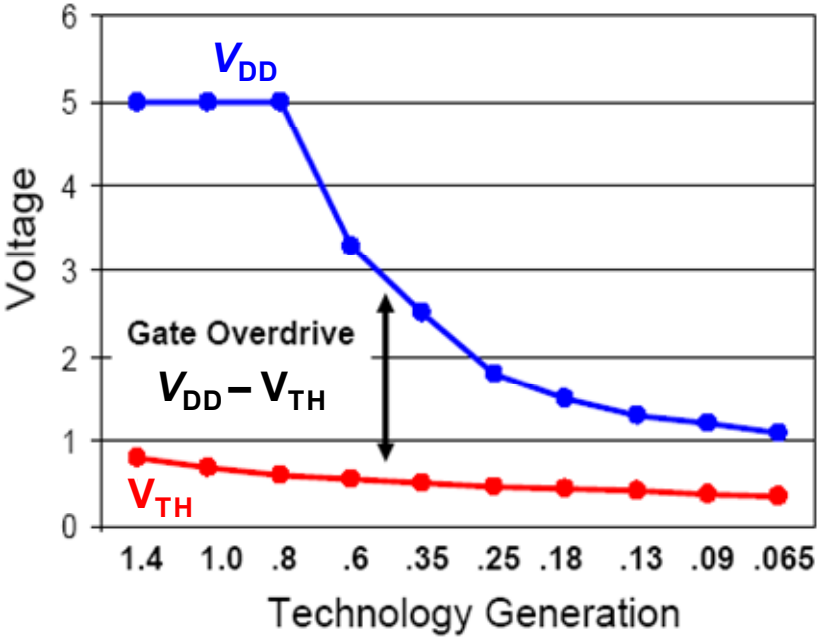
The CMOS Power Crisis

The CMOS Power Crisis

- Due to off-state leakage, V_{TH} cannot be scaled down aggressively. Thus, the supply voltage (V_{DD}) has not been scaled down in proportion to the MOSFET channel length.

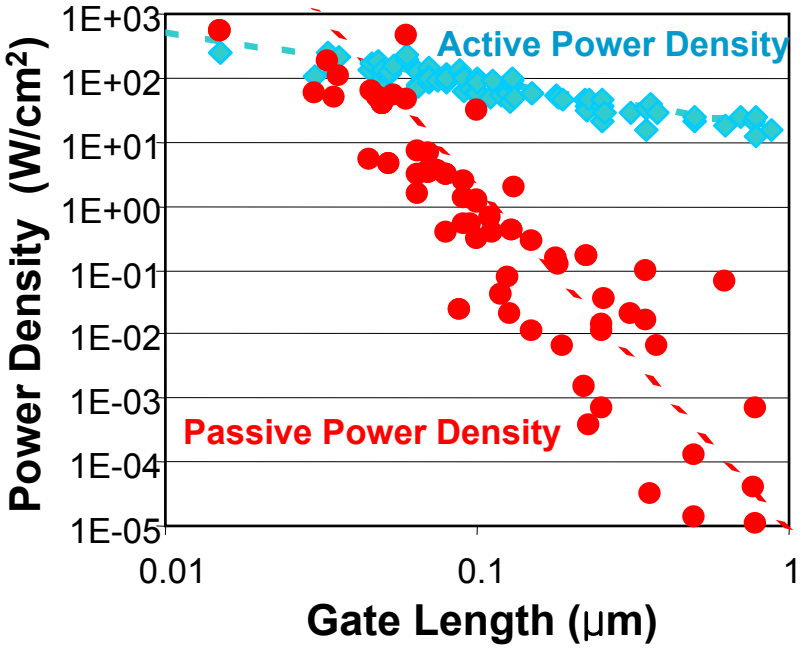
→ CMOS power density has increased with transistor scaling!

CMOS Voltage Scaling



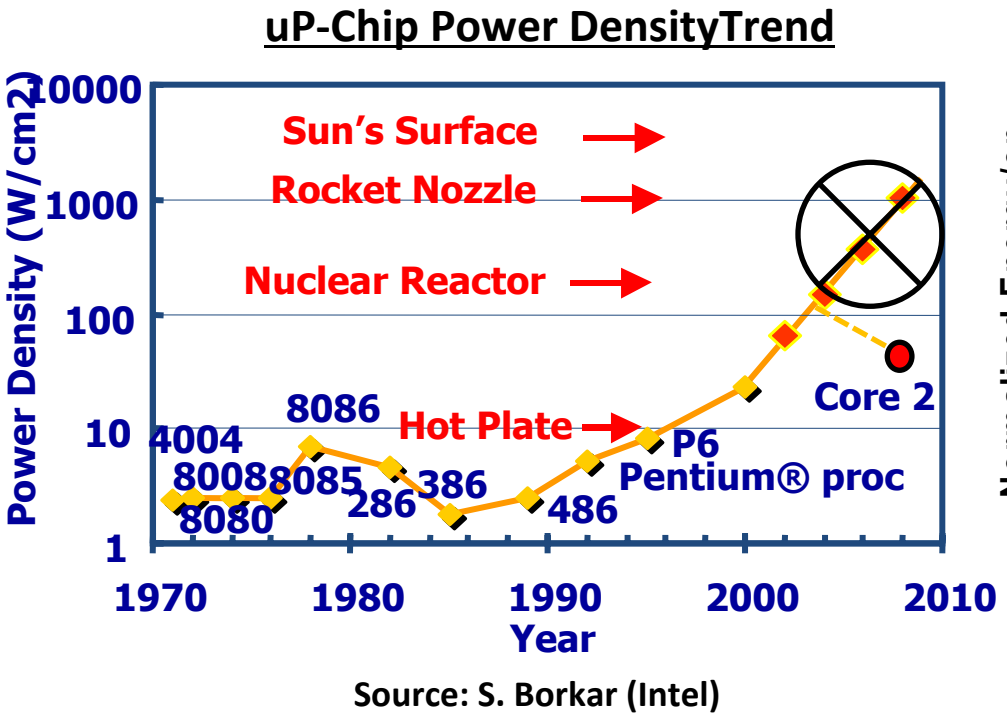
Source: P. Packan (Intel), 2007 IEDM Short Course

Power Density with CMOS Scaling

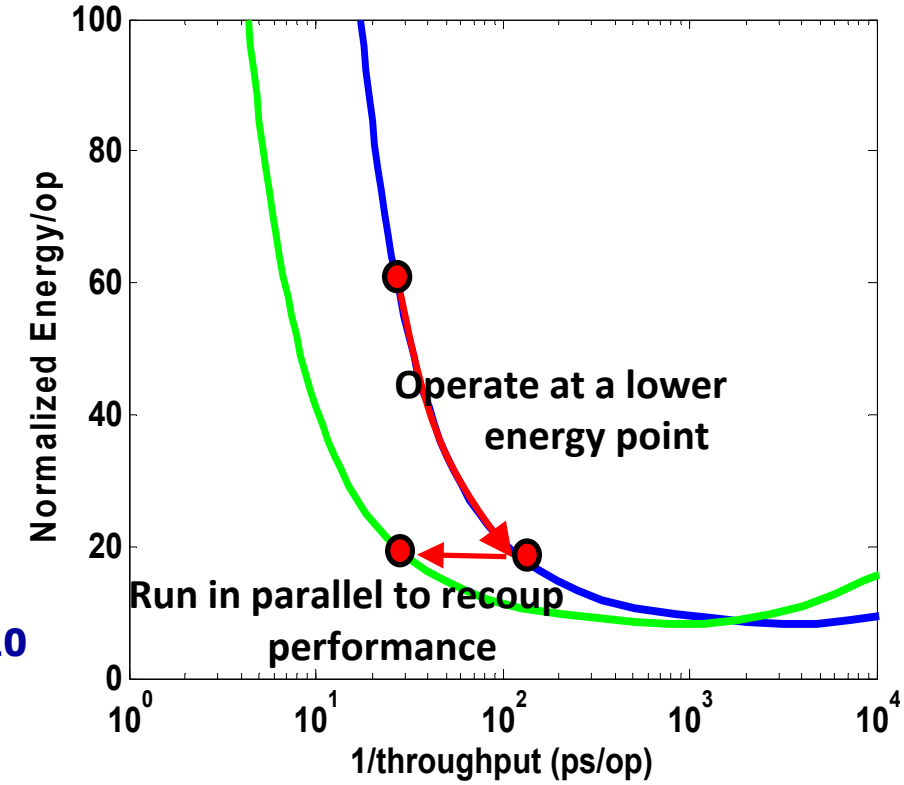


Source: B. Meyerson (IBM) Semico Conf., January 2004

Parallelism



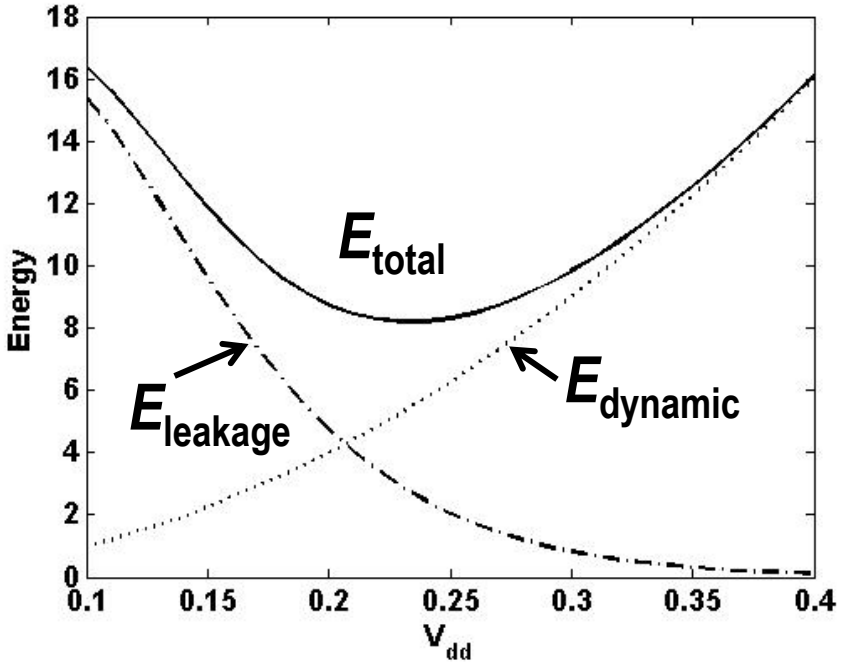
Source: S. Borkar (Intel)



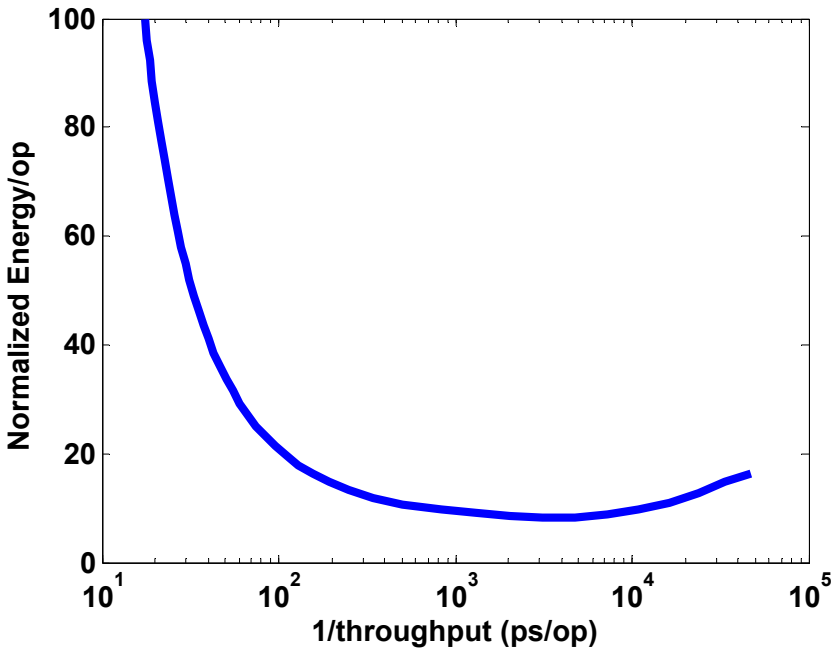
- **Parallelism is the main technique to improve system performance under a power budget.**

Minimizing Operation Energy

CMOS Energy per Operation



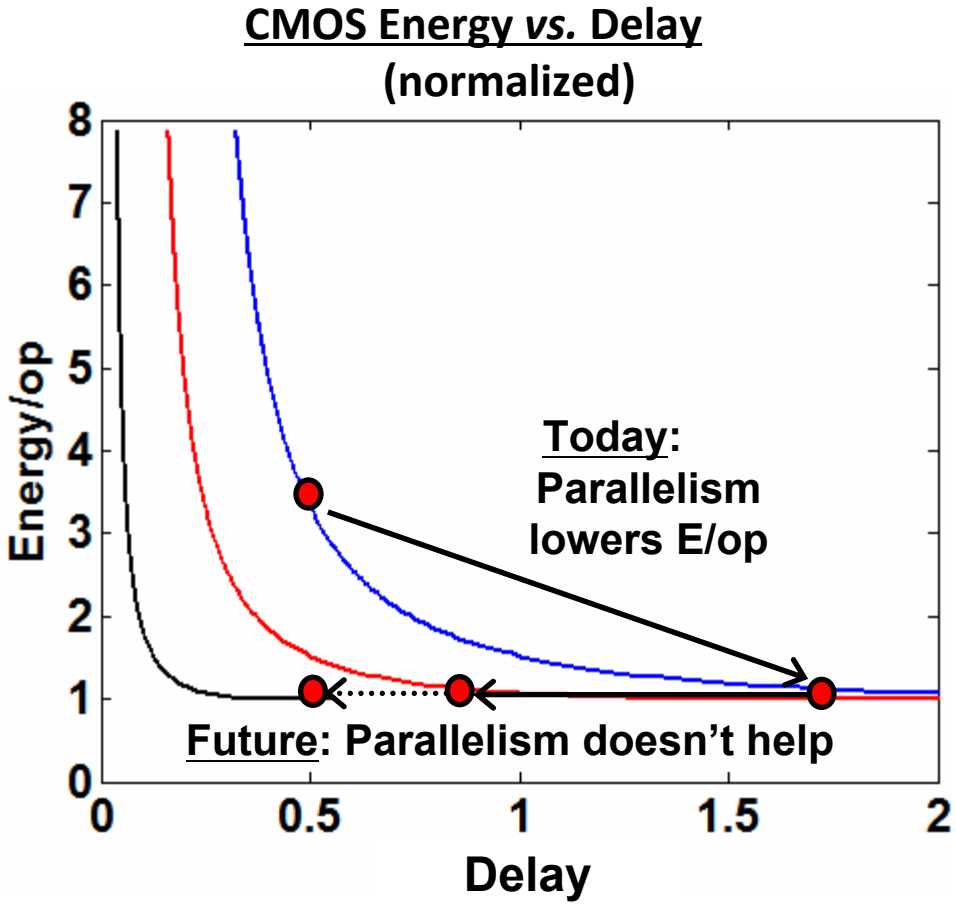
CMOS Energy *vs.* Delay



- $E_{dynamic} + E_{leakage} = \alpha L_d C V_{dd}^2 + L_d I_{OFF} V_{dd} t_{delay}$
  - $t_{delay} = L_d C V_{dd}/(2I_{ON})$

→ **CMOS has a fundamental lower limit in energy per operation, due to subthreshold leakage.**

The Need for a New Switch

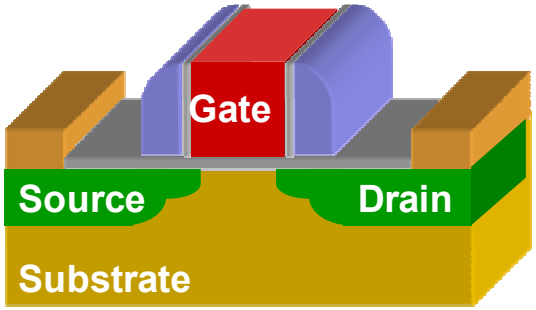


- **When each core operates at the minimum energy, increasing performance requires more power.**

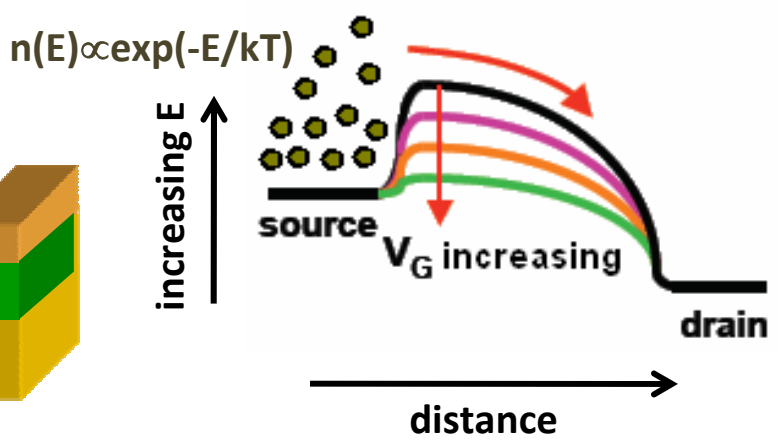
New Switching Devices

MOSFET Subthreshold Swing

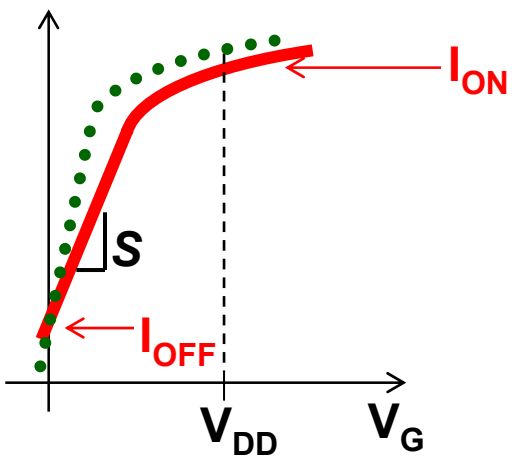
MOSFET Structure:



Electron Energy Band Profile



log I_D

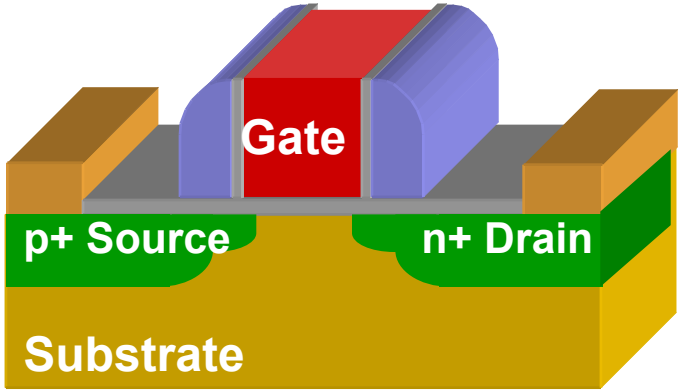


- **In the subthreshold region ($V_{GS} < V_{TH}$),** $I_D \propto \exp\left(\frac{qV_{GS}}{nkT}\right)$
  → **S ≥ 60mV/dec at room temperature**

- **S must be reduced in order to achieve the desired I_{ON}/I_{OFF} with smaller V_{DD}**

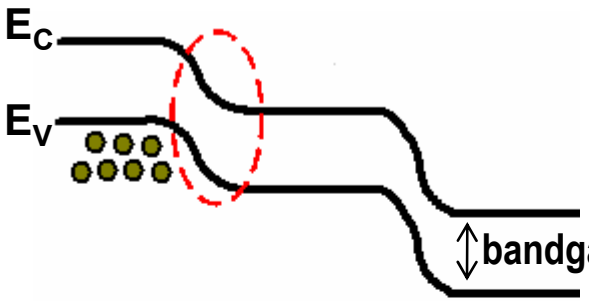
Tunnel FET (TFET)

Structure:

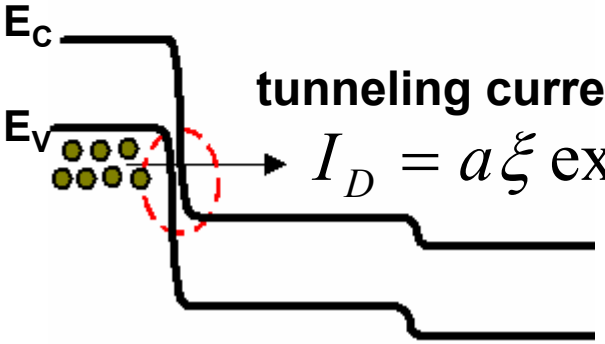


Energy-band Diagrams:

OFF STATE:



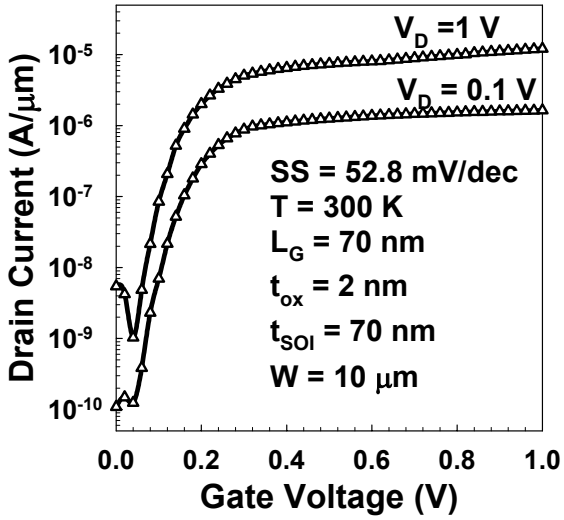
ON STATE:



$$I_D = a\xi \exp(-b/\xi)$$

Si TFET *I-V* Characteristics

W. Y. Choi *et al*. (Seoul Nat'l U. & UC Berkeley)
IEEE-EDL vol. 28, pp. 743-745, 2007



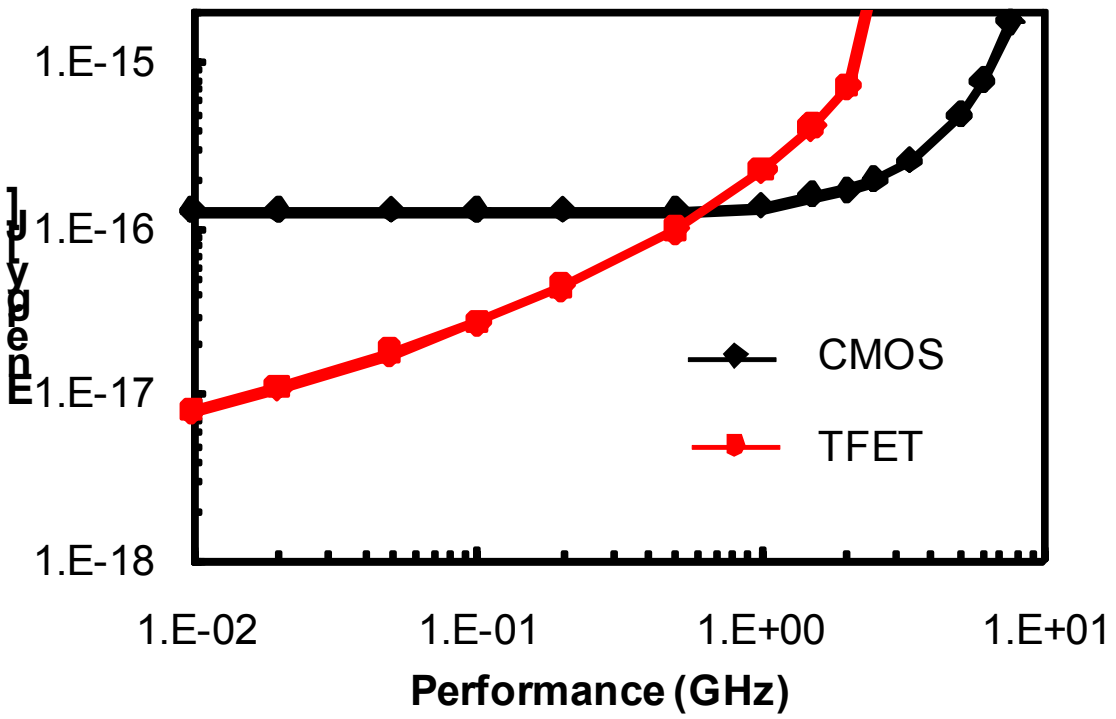
$$\xi = \frac{\left|V_{GS} + V_{tunnel}\right|}{\kappa T_{ox}}$$

$$a \propto A\sqrt{m^*/E_g}$$

$$b \propto \sqrt{m^*/E_g^3}$$

Energy-Performance Comparison

H. Kam *et al*. (UCB, Stanford U.), *2008 IEDM*



30-stage 65nm CMOS inverter chain
(transition probability=0.01, capacitance per stage=2.4fF)

- **Si TFETs appear promising for sub-1GHz applications**

TFET Technology Challenges

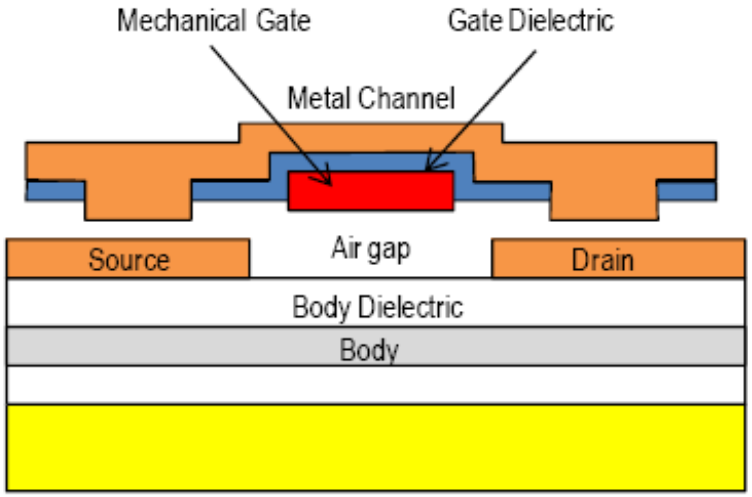
- **Increased I_{ON} to expand range of applications**
  - Advanced semiconductor materials to achieve smaller effective E_g
- **V_{TH} control**
- **TFET-based integrated-circuit design**

MOSFET-Inspired Relay

F. Chen *et al.* (MIT, UCB, UCLA), *2008 ICCAD*

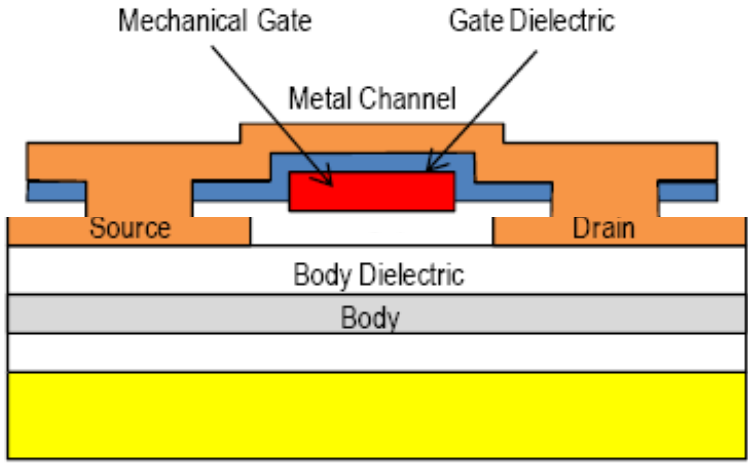
OFF-state

$|V_{GB}| < V_{TH}$



ON-state

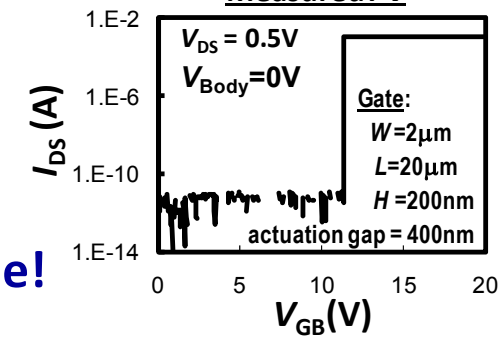
$|V_{GB}| \geq V_{TH}$



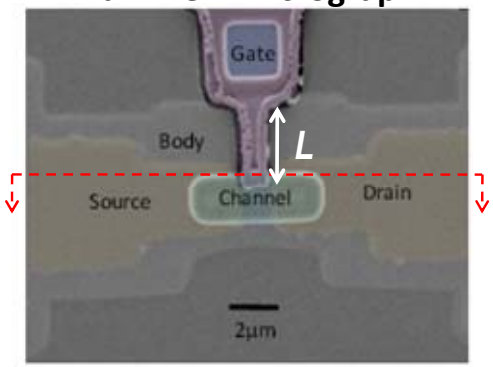
- The mechanical *gate* is electrostatically actuated by a voltage applied between the gate and *body* electrode, to bring the channel into contact with the *source* and *drain* electrodes.
- Ideal switching behavior:
  - Zero off-state leakage
  - Abrupt turn-on

  → low V_{TH} (and V_{DD}) possible!

Measured *I-V*



Plan-View Micrograph

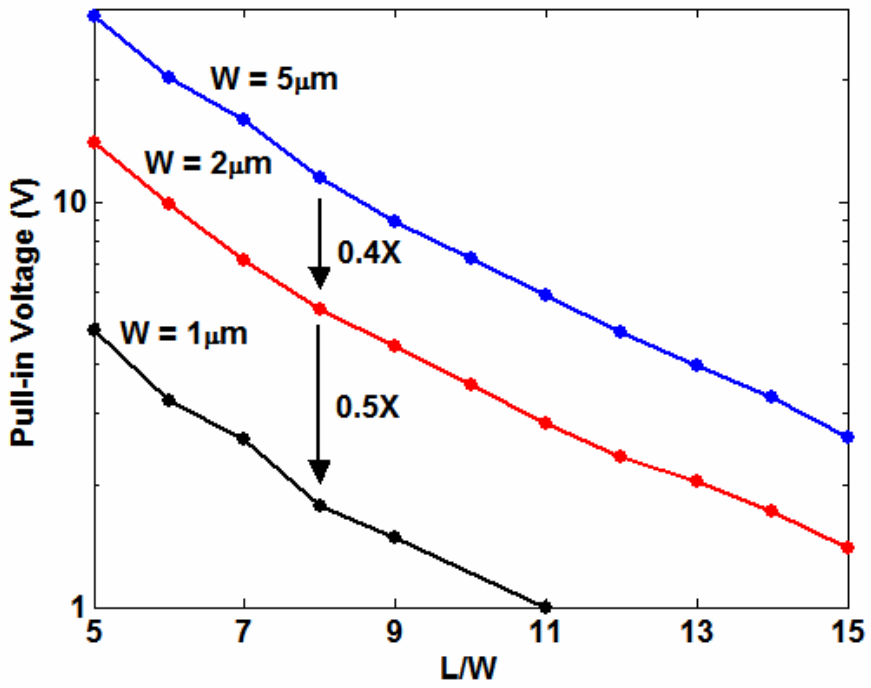


Relay Scaling

F. Chen *et al*. (MIT, UCB, UCLA), *2008 ICCAD*

- **Scaling has similar benefits for relays as for MOSFETs.**

Pull-in Voltage with Beam Scaling



- **Measured pull-in voltages scale linearly**

  $\{W,L,t_{gap}\}$ = {90nm,2.3um,10nm}
  → V_{pi} = 200mV

- **Mechanical delay also scales linearly** (~10ns @ 90nm)

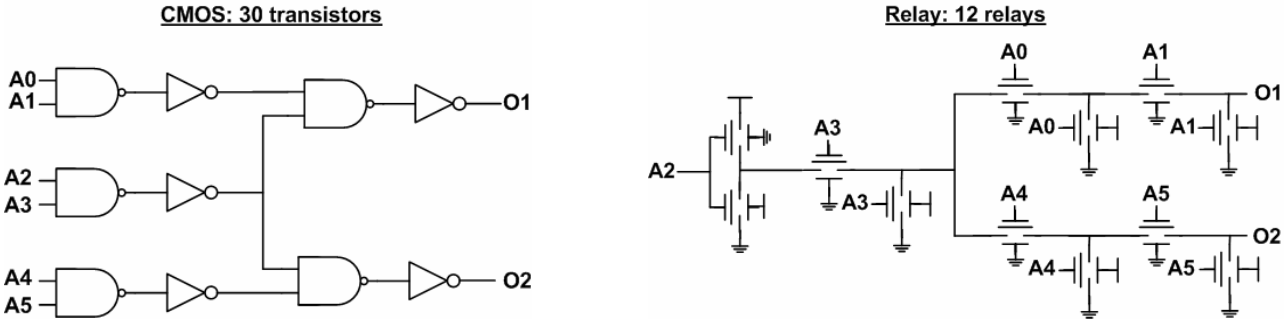
Relay-Based Circuit Design

F. Chen *et al.* (MIT, UCB, UCLA), *2008 ICCAD*

- **Relays have small RC delay but large mechanical delay**

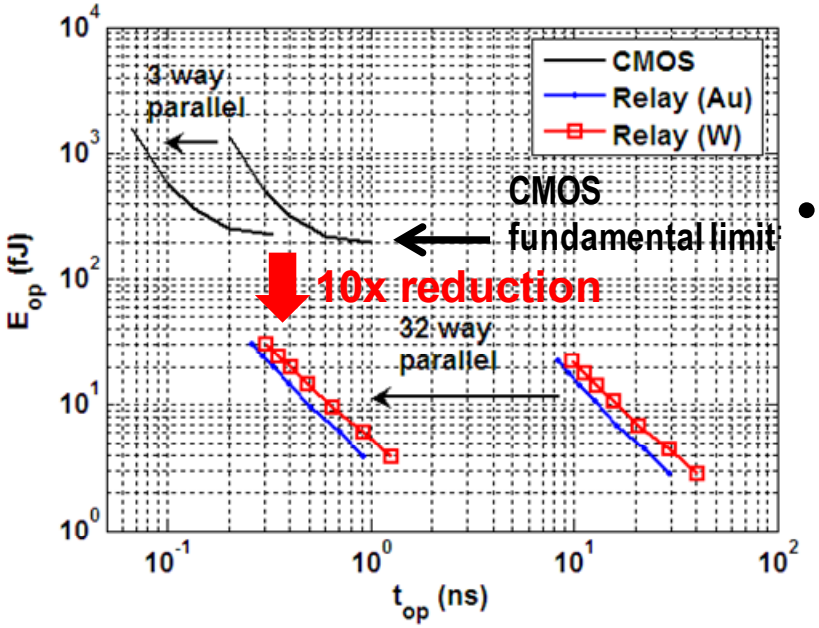
  → Complete all logic in a single complex (pass transistor) gate

Example of CMOS to Relay Logic Mapping:



Energy *vs.* Delay Comparison:

(32-bit adders, 90nm technology)

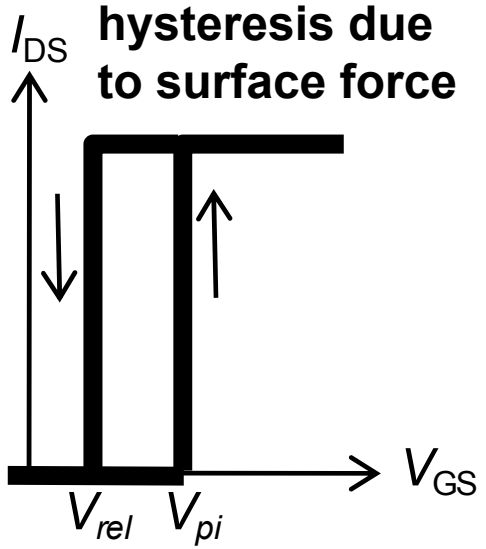


- **A relay adder can be ~10x more energy efficient at the same delay as a CMOS adder.**

Relay Technology Challenges

- **Surface adhesion force**
- **Mechanical contact resistance**
- **Reliability**

Relay *I-V* Characteristic



Summary

Summary

- **Due to subthreshold leakage, CMOS technology has a fundamental limit in energy efficiency.**
- **New switching devices with steeper switching behavior are needed to achieve lower energy per operation.**
  - Examples: tunnel FET, relay
  - Note: Such devices may have very different characteristics than the MOSFET. Thus, they will require new circuit and system architectures to fully realize their potential energy-efficiency (and hence performance) benefits.

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